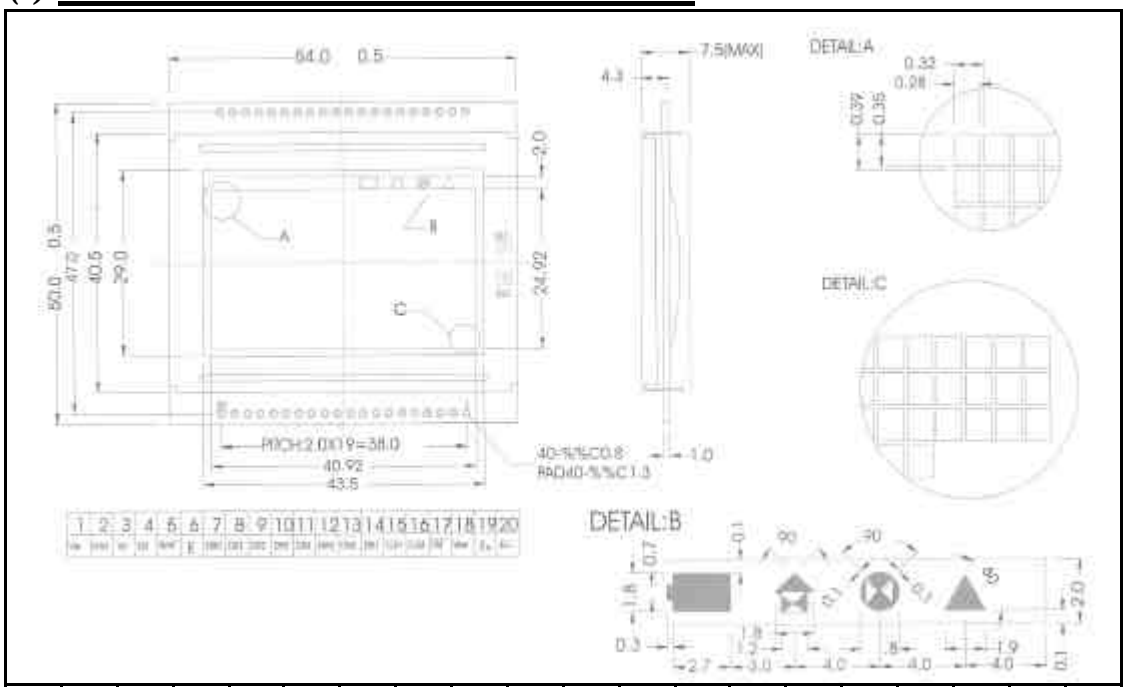
Datasheet For LCD Module – LKG-128064-D2

(1) General Specifications

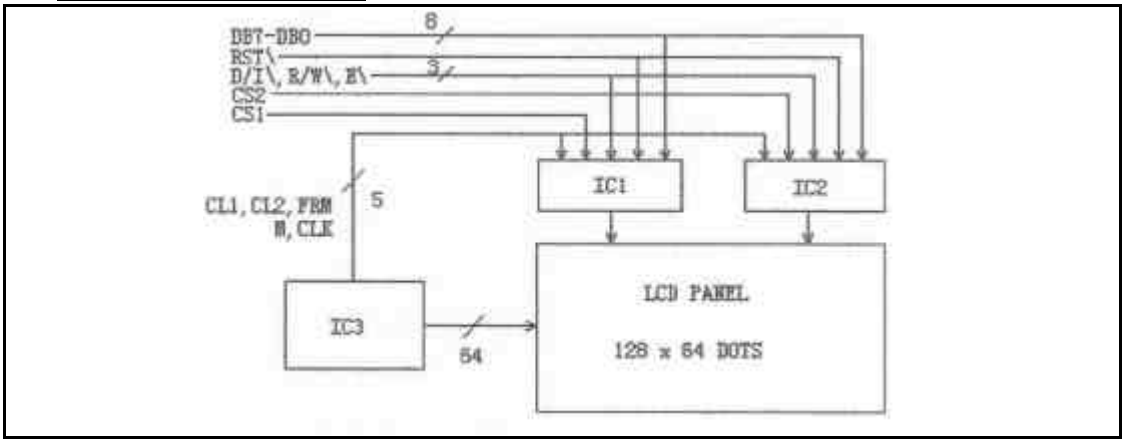
1.1	Display mode	: STN yellow green
1.2	Pixel color	: Black
1.3	Background color	: Yellow green
1.4	Polarizer type	: +ve Transflective
1.5	Viewing angle	: 6:00
1.6	Driving method	: 1/64 duty, 1/6 bias
1.7	Backlight	: Blue EL
1.8	Controller	: KS0108
1.9	Data Transfer	: 8 bit parallel
1.10	EL Driver	: Built in
1.11	Operating temp.	: 0 - 50° C
1.12	Storage temp.	: -20 - 60° C
1.13	Resolution	: 128 columns x 64 rows
1.14	–ve Voltage Generator	: Built in
1.15	Evaluation Board	: LKEB-G02-A (Optional)
1.16	Graphic Software	: BHC128064MP1-0.1 (Optional)

(2) Mechanical Dimensions and Electrical Pin Out



1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Vss	V_{DD}	Vo	D/I	R/W	E	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	CS1	CS2	RES	V_{EE}	EL1	EL2

(3) Circuit Block Diagram



(4) Absolute Maximum Ratings

Item	*Symbol*	*Min.*	*Max.*	*Unit*	*Remark*
Power Supply Voltage	V_{DD} - GND	-0.3	7.0	V	Allowable
LCD Driving Voltage	V_{LCD}	-0.3	17.0		
Operating Temperature Range	T_{op}	0	+50	°C	No Condensation
Storage Temperature Range	T_{st}	-20	+60		

(5) Electrical Characteristics

Item		*Symbol*	*Min.*	*Typ.*	*Max.*	*Unit*
Supply Voltage (Logic)		V_{DD} – GND	4.5	5.0	5.5	V
Supply Voltage (LCD drive)		V_{LCD}	-	9.1	-	V
Supply Voltage (25 °C)		V_O	-	-4.1	-	V
Input Signal Voltage	High	V_{IH} (V_{DD} = 5.0V)	0.7 V_{DD}	-	V_{DD}	V
	Low	V_{IL} (V_{DD} = 5.0V)	0.0	-	0.3 V_{DD}	V

(6) Pin Out Description

Pin Number	*Symbol*	*Level*	*Description*
1	V_{SS}	0 V	Ground
2	V_{DD}	5.0 V	Supply voltage for logic and LCD (+)
3	V_O	Var. V	Contrast adjustment by different voltage
4	D/I	H/L	Data (H) and command (L) register
5	R/W	H/L	Read/Write select signal
6	E	H, H® L	H : Chip enable, H® L : Data write into or read from
7	DB0	H/L	Data bit 0
8	DB1	H/L	Data bit 1
9	DB2	H/L	Data bit 2
10	DB3	H/L	Data bit 3
11	DB4	H/L	Data bit 4
12	DB5	H/L	Data bit 5
13	DB6	H/L	Data bit 6
14	DB7	H/L	Data bit 7
15	CS1	H/L	Chip select signal for left screen, CS1=0 & CS2=1
16	CS2	H/L	Chip select signal for right screen, CS1=1 & CS2=0
17	RES	L® H	Reset the system (Keep at 1 after reset)
18	V_{EE}	-4.1 V	Output from built in –ve voltage generator
19	EL1	H/L	(H) EL off, (L) EL on
20	EL2	NC	No connection

(7) MCU Interface

The LKG-128064-D2 uses 8 bits of bi-directional data bus (D0-D7) to transfer data. The reset pin must be set from low to high to reset the module and keep at high during the operation.

7.1 Register

Both input register and output register are provided to interface to an MCU whose speed is different from that of internal operation. The selection of these registers depend on the combination of R/W and D/I signals as following table :

D/I	R/W	Operation
1	1	Reads data out of output register as internal operation (display data RAM → output register)
1	0	Writes data into input register as internal operation (input register → display data RAM)
0	1	Busy check. Read of status data.
0	0	Instruction

7.2 Busy Flag

Busy flag being "1" indicates that the KS0108 is performing its internal operation and any instruction other than Read Status is disabled. The busy flag is output to pin DB7 by a Read Status instruction.

7.3 Display On/Off Flip Flop

The display on/off flip flop selects one of two states, on state and off state of segments Y1 to Y64. In on state, the display data corresponding to that in RAM is output to the segments. On the other hand, the display data at all segments disappear in off state independent of the data RAM. It is controlled by display on/off instruction. RES signal = 0 sets the segments in off state. The status of the flip flop is output to DB5 by status read instruction. Display on/off instruction does not influence data RAM.

7.4 Display Start Line Regsister

The display start line register specifies the line in RAM which corresponds to the top line of LCD panel, when displaying contents in display data RAM on the LCD panel. It is used for scrolling of the screen.

6-bit display start line information is written into this register by the display start line set instruction.

7.5 X, Y Address Counter

A 9-bit counter which designates addresses of the internal display data RAM. X address counter (upper 3 bits) and Y address counter (lower 6 bits) should be set to each address by the respective instructions.

1. **X address counter**

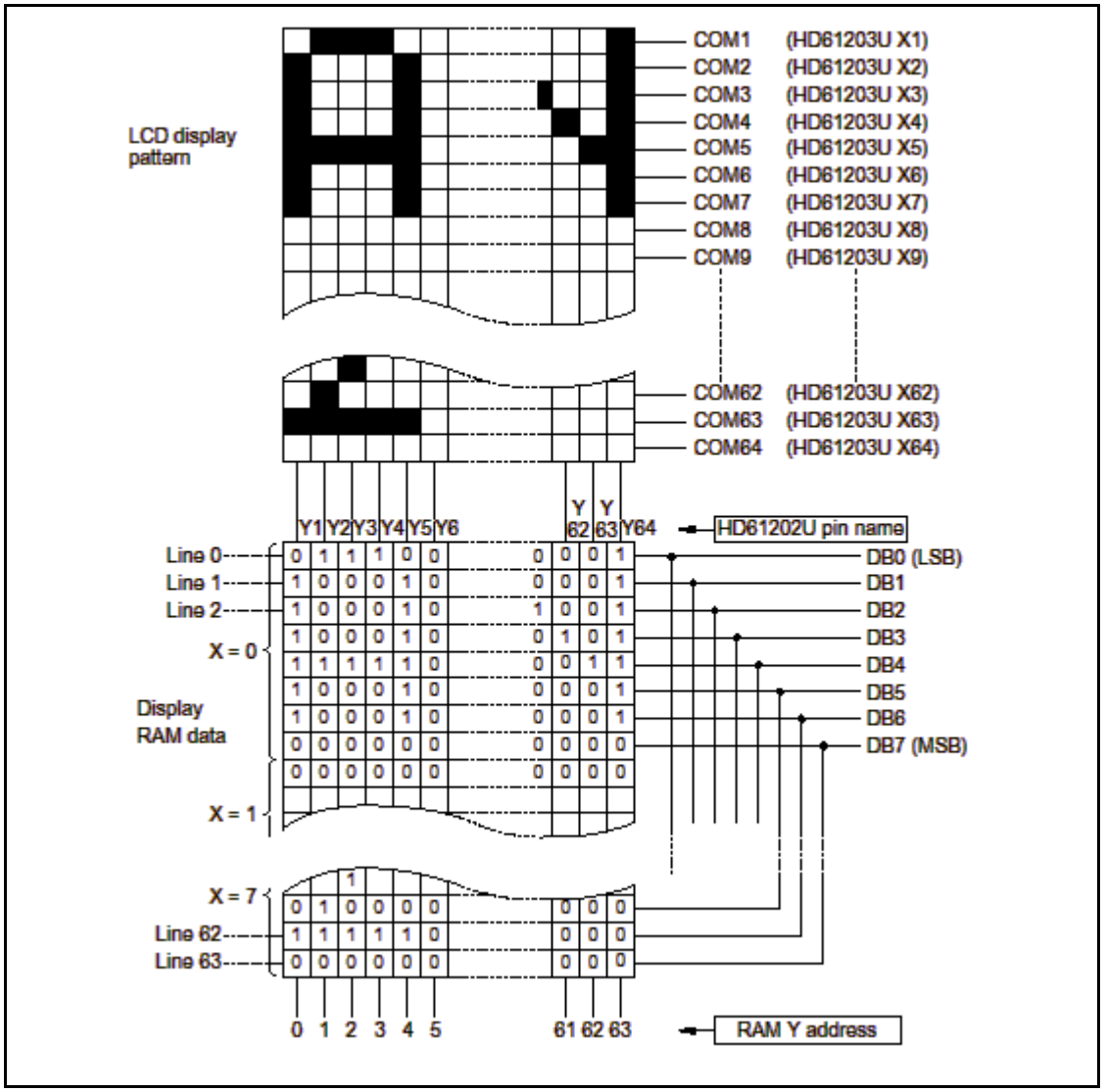
   Ordinary register with no count functions. An address is set by instruction.

2. **Y address counter**

   An address is set by instruction and is increased by 1 automatically by R/W operations of display data. The Y address counter loops the values of 0 to 63 to count.

7.6 Display Data RAM

Stores dot data for display. 1-bit data of this RAM corresponds to light on (data = 1) and light off (data =0) of 1 dot in the display panel.



7.7 Reset

The system can be initialized by setting RES pin at low level when turning power on.

1. **Display off**
2. **Set display start line register line 0.**

   While RES is low level, no instruction except status read can be accepted. Therefore, execute other instructions after making sure that DB4=0 (clear RESET) and DB7=0 (ready) by status read instruction.

(8) Display Control Instructions

Instructions	Code R/W	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Functions	
Display on/off	0	0	0	0	1	1	1	1	1	1/0	Controls display on/off. RAM data and internal status are not affected. 1: on, 0: off.	
Display start line	0	0	1	1	Display start line (0–63)						Specifies the RAM line displayed at the top of the screen.	
Set page (X address)	0	0	1	0	1	1	1	Page (0–7)			Sets the page (X address) of RAM at the page (X address) register.	
Set Y address	0	0	0	1	Y address (0–63)						Sets the Y address in the Y address counter.	
Status read	1	0	Busy	0	ON/ OFF	Reset	0	0	0	0	Reads the status. RESET 1: Reset 0: Normal ON/OFF 1: Display off 0: Display on Busy 1: Internal operation 0: Ready	
Write display data	0	1	Write data								Writes data DB0 (LSB) to DB7 (MSB) on the data bus into display RAM.	Has access to the address of the display RAM specified in advance. After the access, Y address is increased by 1.
Read display data	1	1	Read data								Reads data DB0 (LSB) to DB7 (MSB) from the display RAM to the data bus.	

Note: Busy time varies with the frequency (f_{CLK}) of ø1, and ø2.
($1/f_{CLK} \leq T_{BUSY} \leq 3/f_{CLK}$)

The above table shows the instructions. Read/write (R/W) signal, data/instruction (D/I) signal, and data bus signals (DB0 to DB7) are also called instructions because the internal operation depends on the signals from the MCU.

These explanations are detailed in the following pages. Generally, there are three kinds of instructions :

1. **Instruction to set addresses in the internal RAM**
2. **Instruction to transfer data from/to the internal RAM**
3. **Other instructions**

In general use, the second type of instruction is used most frequently. Since Y address of the internal RAM is increased by 1 automatically after writing (reading) data, the program can be shortened. During the execution of an instruction, the system cannot accept instructions other than status read instruction. Send instructions from MCU after making sure that the busy flag is 0, which is proof that an instruction is not being executed.

8.1 Display On/Off

	R/W	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	1	1	1	1	1	D
			MSB							LSB

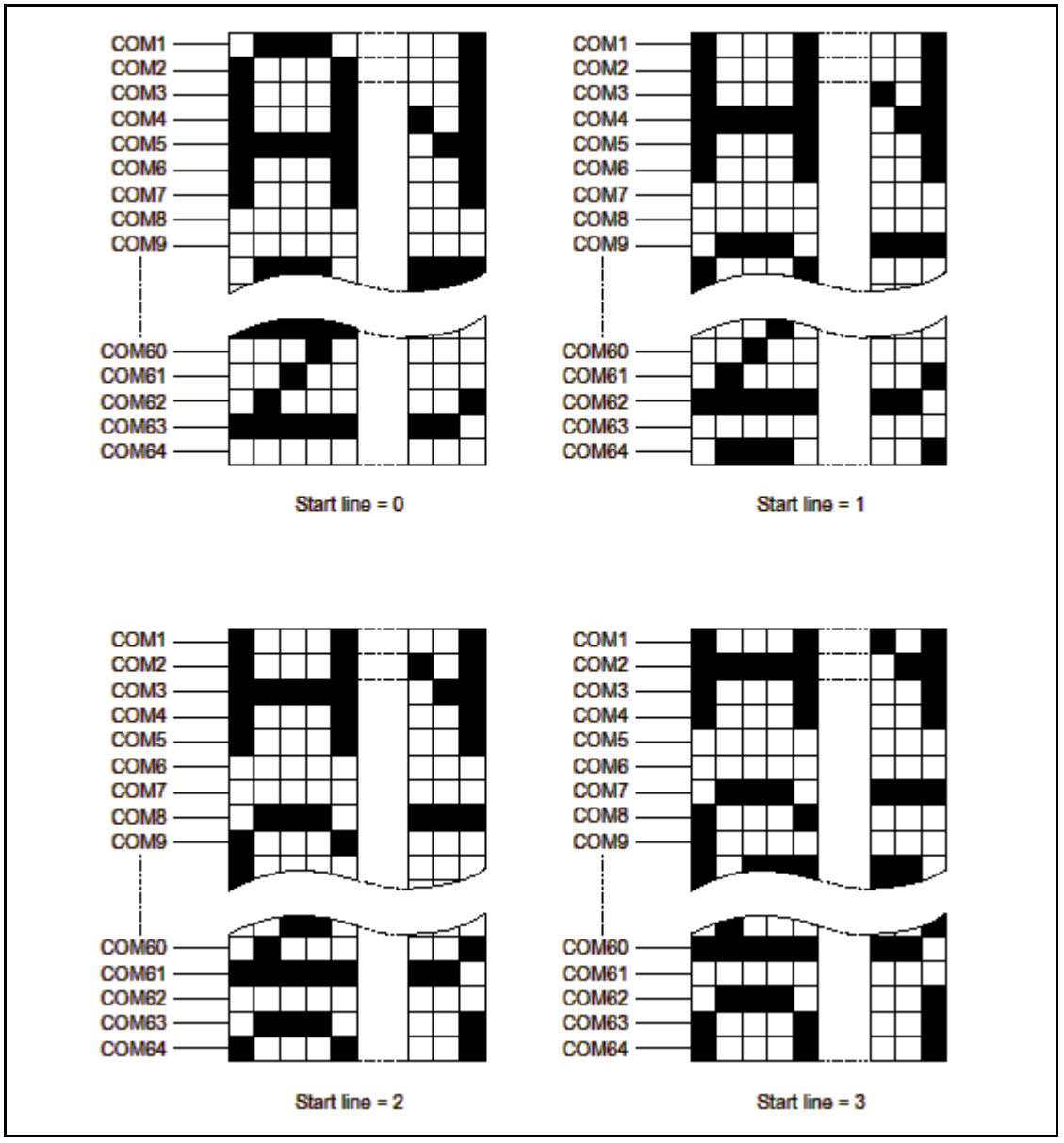
The display data appears when D is 1 and disappears when D is 0. Though the

data is not on the screen with D=0, it remains in the display data RAM. Therefore, you can make it appear by changing D=0 into D=1.

8.2 Display Start Line

	R/W	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	1	A	A	A	A	A	A
			MSB							LSB

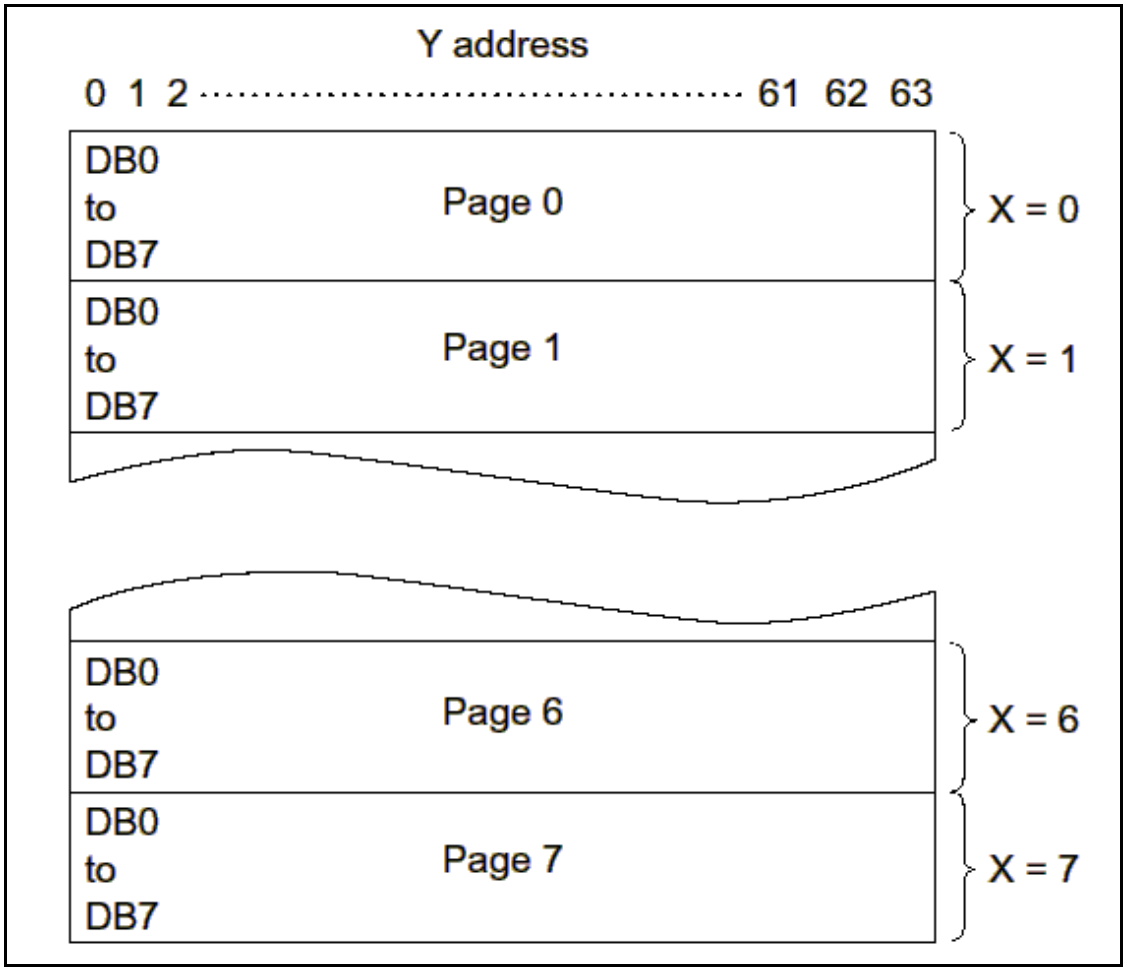
Z address AAAAAA (binary) of the display data RAM is set in the display start line register and displayed at the top of the screen. The following figure shows examples of display when the start line = 0-3.



8.3 Set Page (X Address)

	R/W	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	0	1	1	1	A	A	A
			MSB							LSB

X address AAA (binary) of the display data RAM is set in the X address register. After that, writing or reading to or from MCU is executed in this specified page until the next page is set.



8.4 Set Y Address

	R/W	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	1	A	A	A	A	A	A
			MSB							LSB

Y address AAAAAA (binary) of the display data RAM is set in the Y address counter. After that, Y address counter is increased by 1 every time the data is written or read to or from MCU.

8.5 Status Read

	R/W	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	0	Busy	1	On/Off	RESET	0	0	0	0
			MSB							LSB

Busy :

When busy is 1, the LSI is executing internal operations. No instructions are accepted while busy is 1, so you should make sure that busy is 0 before writing the next instructions.

On/Off :

Shows the liquid crystal display conditions : on condition or off condition.

When on/off is 1, the display is in off condition.

When on/off is 0, the display is in on condition.

RESET :

RESET = 1 shows that the system is being initialized. In this condition, no instructions except status read can be accepted.

RESET = 0 shows that initializing has finished and the system is in the usual operation condition.